REMARKS

The Applicants request reconsideration of the rejection.

Claims 1-4, 6-7, 9 and 11-13 will be pending upon entry of the foregoing amendments.

Claims 1, 3-5, 7, and 9-15 were objected to as containing the alleged informalities set forth on pages 3-4 of the Office Action. The claims have been amended to address the Examiner's concerns.

Claims 1-3 and 8 were rejected under 35 U.S.C. §102(e) as being anticipated by Cheng, et al., US 6,367,060 (Cheng). The Applicants traverse as follows.

An important feature of the present invention is that the timing of a clock signal inputted into a flip-flop is adjusted by using different kinds of adjusting methods (Figs. 2 to 4) such as detour wiring, insertion of a delay element, or increase of the number of fan-outs.

In contrast, Cheng employs a plurality of buffer types with different load driving abilities as a single method of adjusting a clock signal inputted into a register (column 5, lines 24-35). Each buffer type has associated with it a propagation delay, and each buffer type impacts clock transition times at the registers by a certain amount (column 5, lines 36-38).

More particularly, the clock tree synthesizer inputs data including component placement and timing constraints for a circuit design (410 of Fig. 4, column 4, lines 31-37), then recognizes all leaf nodes included in the clock tree (420 of Fig. 4, column 5, lines 6-11), and calculates the balanced cluster sets of the leaf nodes based on the available buffer types (430 of Fig. 4, column 5, lines 24-35). Then, each calculated cluster set is tested against a design constraint (clock transition time, etc.) (440 of Fig. 4, column 6, lines 5-13), and any cluster set that does not meet the timing constraint is removed from consideration (445 of Fig. 4, column 6, lines 14-24), while a cost is calculated for cluster sets that met the timing constraint (450 of Fig. 4, column 6, lines 25-44) and a cluster having the lowest calculated cost is selected (455 of Fig. 4, column 6, lines 45-53).

Further, additional design constraints are tested (the cumulative propagation delay from the root node to the registers, etc.) (470 of Fig. 4, column 7, lines 21-29). If the additional design constraints are not met, different buffer types are selected, and the cost equation is adjusted and the process returns to block 420 (475 of Fig. 4, column 7, lines 21-29).

In this respect, the cost is equal to the cumulative area necessary for inserting the set of buffers, plus a cost factor, times the propagation delay for the buffer type (column 6, lines 25-44), wherein each of the cumulative area and the cost factor relates to the buffer type.

In sum, Cheng relates marginally to the invention in eliminating clock skew between registers, but employs one adjusting method (a plurality of buffer types with different driving abilities of a load) (column 5, lines 36-47) instead of the multiple-method technique of the present invention, in which the timings of a clock signal are adjusted by using different kinds of adjusting methods.

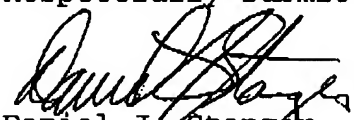
The adjusting method of Cheng using the buffer types seems to correspond to the method shown in Fig. 2C of the present application. That is, Cheng merely discloses one of the plurality of adjusting methods of the present invention.

Moreover, in Cheng, the clock tree synthesizer is arranged in a manner that the clock tree is tested for setup time and/or hold time violations even if the tested design constraints are met (480 of Fig. 4, column 8, lines 25-27), and register positions are changed in the clock tree as needed (490 of Fig. 4, column 8, lines 27-30). This processing is not for the processing for the design constraint and so does

not relate to the timing adjusting method for a clock signal of the present invention.

In view of the foregoing amendments and remarks, the Applicants request reconsideration of the rejection and allowance of the claims.

Respectfully submitted,



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